AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A duplex device, comprising:

an active module having a primary central processing unit that carries out control and data processes, a primary arbiter that arbitrates the use of a primary bus, a primary memory controller that controls access to a primary memory, a primary D-channel controller that provides a primary first-in first-out (FIFO) memory for the communication of parallel data on a duplexing path, and a primary C-channel controller, separate from the primary D-channel controller, that communicates primary status information of the active module;

a standby module having a secondary central processing unit that carries out control and data processes, a secondary arbiter that arbitrates the use of a secondary bus, a secondary memory controller that controls access to a secondary memory, a secondary D-channel controller that provides a second FIFO memory for the communication of the parallel data on the duplexing path, and a secondary C-channel controller, separate from the secondary D-channel controller, that communicates secondary status information of the standby module;

a C-channel provided between the active module and the standby module that exchanges the primary and secondary status information between the primary and secondary C-

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